**Introduction**

The purpose of this lab is to design a sequential circuit to control the operation of a vending machine which dispenses a $0.25 product

The circuit has three inputs, N (nickel), D (dime), Q (quarter), and two outputs, P (product) and C (change).

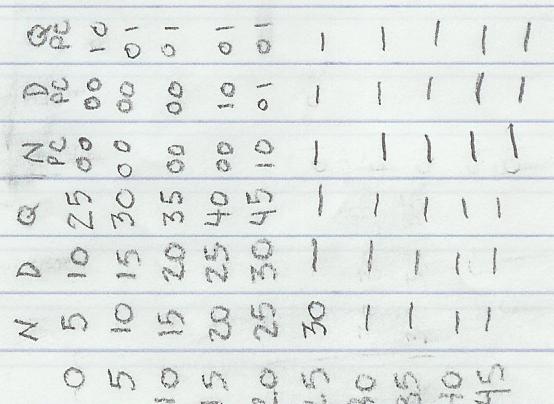
**Preliminary**

1. **Define the states**

The states consist of how much money is currently inside the soda machine.  
states: 0,5,10,15,20,25,30,35,40,45

1. **Write the state table**

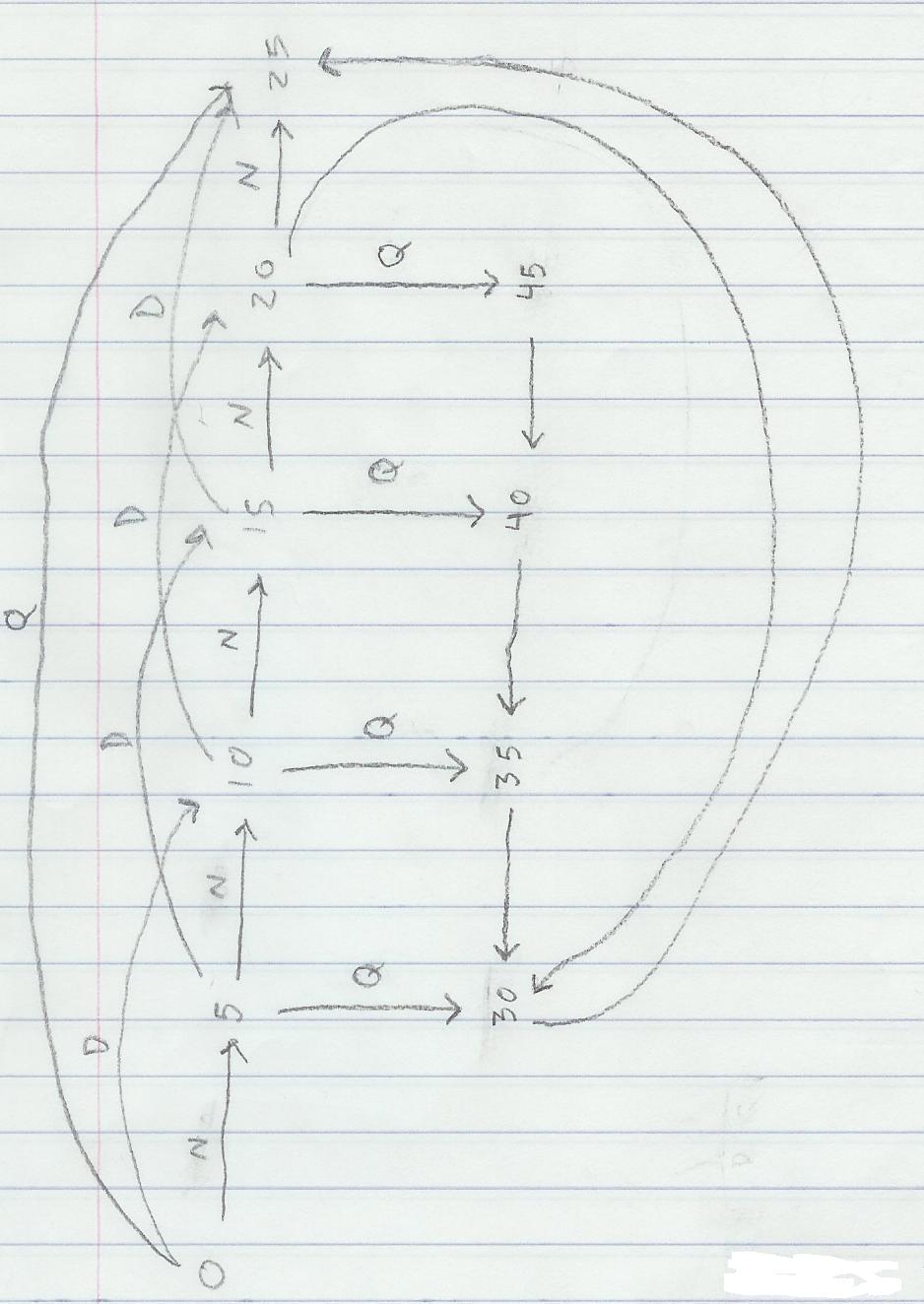
To create the state table I had to find the output of every possible combination of coins.



Note: The areas marked with a dash never occur because only one coin can be inputted at a time.

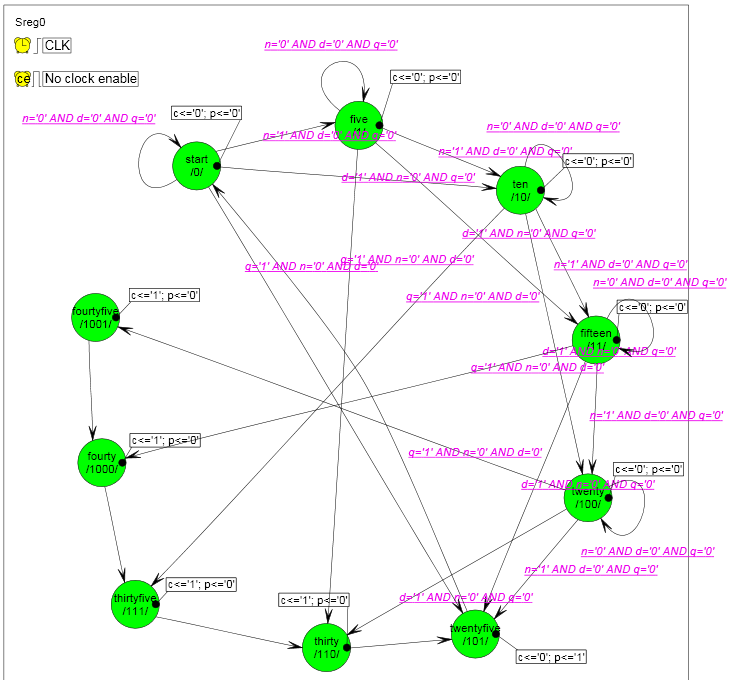
1. **Develop the state diagram**

The state table was then easily tranlated into a state diagram.



**Lab Work**

After we created the state diagram we had to input it into Aldec.



1. **Develop VHDL for the state machine**

No equations or stimulus was required for this lab since all of the logic resided inside the GAL chip. Here is the test bench anyhow.

library ieee;

use ieee.std\_logic\_unsigned.all;

use ieee.std\_logic\_arith.all;

use ieee.std\_logic\_1164.all;

entity lab7l\_tb is

end lab7l\_tb;

architecture TB\_ARCHITECTURE of lab7l\_tb is

-- Component declaration of the tested unit

component lab7l

port(

CLK : in std\_logic;

D : in std\_logic;

N : in std\_logic;

Q : in std\_logic;

C : out std\_logic;

P : out std\_logic );

end component;

-- Stimulus signals - signals mapped to the input and inout ports of tested entity

signal CLK : std\_logic;

signal D : std\_logic;

signal N : std\_logic;

signal Q : std\_logic;

-- Observed signals - signals mapped to the output ports of tested entity

signal C : std\_logic;

signal P : std\_logic;

begin

-- Unit Under Test port map

UUT : lab7l

port map (

CLK => CLK,

D => D,

N => N,

Q => Q,

C => C,

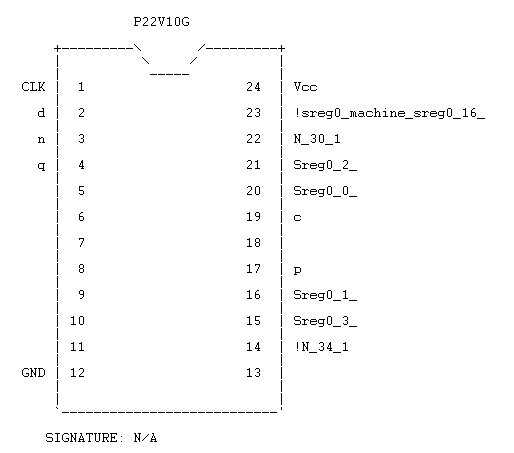
P => P

);

end TB\_ARCHITECTURE;

1. **Synthesize the JEDEC file**

We then synthesized the vhdl, programmed the GAL and used this chip diagram to create the circuit.



1. **Develop the circuit diagram**

Only the GAL chip was used, so the JED file serves as the circuit diagram.

1. **Develop the wire list**

Again, because only one chip was used, the wire list can be visualized from the GAL chip diagram.

power - vcc, gnd

inputs - d, n, q

outputs - p,c

clock - clk

pins 14,15,16,20,21,22,23 are disregarded.

1. **Assemble the circuit**

I assembled the circuit, and it seemed to work although I did not have much time to tinker with it. I saw all the results when I was helping my partner. Adding the clock cycle timer was essential to properly add coins and see how much change was returned.